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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,884	11/04/2003	Jason Michael Norman	BUR920030073US1	2883

28722 7590 02/24/2005

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EXAMINER	
WACHSMAN, HAL D	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/605,884	NORMAN ET AL.	
	Examiner	Art Unit	
	Hal D. Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-18* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This application is in condition for allowance except for the following formal matters:

a) The drawings are objected to because labeling (i.e. in words) is needed in Figure 1 so as to facilitate an understanding of the invention from the drawings. Appropriate correction is required.

b) The use of the trademark Verilog (see page 2 of the specification) has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

c) The Brief Description of the Drawings refers to a Figure 5 but there are actually Figures 5a and 5b. Appropriate correction is required.

d) Claims 1-18 are objected to under 37 C.F.R. 1.75(i) because each element or step of the claims are not separated by a line indentation. Appropriate correction is required.

e) Claims 1-18 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1, line 7, cites "said logic area" which it appears should be "said one logic area". This same type of problem also occurs in claim 7, lines 8-9 and claim 13, lines 9-10. Claim 1, line 8, cites "retesting the altered logic area..." however it is not clear in the claim that the altered logic area has been tested a first time before being

retested. This same type of problem also occurs in claim 7, line 10, and claim 13, line 11. Claim 1, lines 8-9, cite "retesting the altered logic area using only with the one or more first testcases..." however using only what with the one or more first testcases ? This same type of problem also occurs in claim 7, lines 10-11, and claim 13, lines 11-12. Claim 2, lines 2-3, cite "..the filed first testcases.." which it appears should be "..the failed first testcases...". This same type of problem also occurs in claim 8, lines 2-3, and claim 14, line 4. Claim 2, line 5, cites "re-running at least one second testcase..." however it is not clear in the claims that at least one second testcase was ran a first time. This same type of problem also occurs in claim 8, line 5, and claim 14, line 6. Claim 2, lines 5-6, cite "..the other logic areas" however the antecedent basis is singular. This same type of problem also occurs in claim 8, line 6, and claim 14, line 7. Claim 4, line 4, cites "second failed testcases" which lacks antecedent basis. This same type of problem also occurs in claim 10, line 4, and claim 16, line 4. Claim 6, line 2, cites "..the circuit" however is this referring to the circuit in one of the logic areas ? This same type of problem also occurs in claim 12, line 2, and claim 18, line 3. The preamble of claim 13 refers to a computer program product residing on a computer usable medium and then the body of the claim refers to the program code however there is ambiguity with respect to how the functionality of the computer program product is being realized if the program code is not being executed on a general purpose computer for example. The examiner asks the applicant to better claim the limitations cited above. While the examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

2. The following references are cited as being art of general interest: Niederer et al. (6,601,229) which disclose testcase development using VHDL for logic verification, Geer et al. (6,212,667) which disclose the running of testcases to test the design of an integrated circuit and Roesner et al. (US 2004/0216077) which disclose configuring a digital system described by a hardware description language model.

3. Claims 1-18 are allowable over the prior art because the prior art does not disclose or suggest: altering a circuit in one logic area of one or more logic areas to create an altered logic area; retesting the altered logic area using one or more first testcases associated with the unaltered logic area; and counting the number of logic areas in identified failed first testcases to predict which logic areas are adversely affected by the altering of the circuit.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D. Wachsman whose telephone number is 571-272-2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
February 22, 2005